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Interface Trap Densities and Admittance Characteristics of III-V MOS capacitors

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High-*k*/III-V interfaces in metal-oxide-semiconductor capacitor structures with $In_{0.53}Ga_{0.47}As$ channels exhibit certain admittance characteristics that are almost universally observed, independent of the specific high-*k* material or deposition technique used. These include a "hump" in the capacitance-voltage curves at negative biases (depletion region) and low frequencies for *n*-type channels, and pronounced frequency dispersion in accumulation. The paper discusses both features in the context of the high density of non-uniformly distributed interface trap states in the semiconductor band gap that is typical of these interfaces.

Introduction

III-V semiconductor surfaces are prone to high interface trap densities (D_{it}), causing the admittance characteristics dielectric/III-V interfaces to be remarkably similar, even when different dielectrics and/or dielectrics deposited by different methods are used (1). The energy distribution of the D_{it} in the semiconductor band gap is likely also very non-uniform. For example, the D_{it} of dielectric/*n*-$In_{0.53}Ga_{0.47}As$ interfaces is sufficiently low to achieve band bending (semiconductor Fermi level movement) in the upper half of the semiconductor band gap under an applied voltage. Here, we discuss some of the general admittance characteristics of metal-oxide-semiconductor capacitor (MOSCAPs) structures with *n*-type $In_{0.53}Ga_{0.47}As$ channels.

Frequency Dispersion at Negative Gate Bias

At negative biases and room temperature, *n*-MOSCAPs with $In_{0.53}Ga_{0.47}As$ typically show an increase in capacitance with decreasing frequency at negative bias (see Fig. 1). In the literature the upturn of capacitance at negative bias has often been explained with a response due to minority carriers (true or weak inversion). However, if minority carrier generation would be responsible for the upturn in capacitance with decreasing frequency at negative biases, then the capacitance should become independent of gate bias. Instead, typical CV curves show a "hump" at negative biases and low frequencies, which is characteristic for interface trap response (1). Recent studies of the activation energy of this hump using temperature-dependent studies have shown that it originates from interface states located 0.1 eV below midgap (2).

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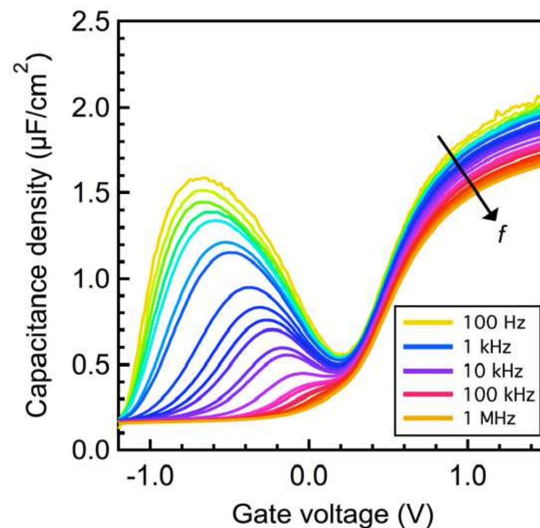

Figure 1: Capacitance-voltage characteristics as a function of measurement frequency of a 3 nm thick $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAP with a Ni top electrode.

Frequency Dispersion at Positive Gate Bias

The origin of the frequency dispersion that is observed in accumulation, for example for the MOSCAP shown in Fig. 1, is currently being debated in the literature. The following mechanisms have been proposed in the literature to explain the frequency dispersion:

- *Interface traps:* the recombination time constants of interface states that line up with the semiconductor Fermi level at positive gate bias are expected to be very short, because the semiconductor Fermi level moves deep into the conduction band (1). Communication of traps with the semiconductor bands is thus *not* expected to give rise to strong frequency dispersion in accumulation.
- *Border traps (3,4,5,6)/disorder near the interface (7):* tunneling from the semiconductor bands into these defects is associated with a time constant that depends on their distance to the interface, giving rise to frequency dispersion. The border trap model is consistent with the experimentally observed temperature independence of the dispersion (3). However, the reported frequency dispersion characteristics of well-behaved dielectric/III-V interfaces with different dielectrics and/or dielectrics deposited by different methods are remarkably similar, which is not expected if defects in the dielectric are responsible for the dispersion. The border trap model is unlikely to explain why dispersion characteristics depend on the dielectric thickness (Fig. 2).
- *Leakage and series resistance (8):* the dispersion is typically observed to very low frequencies [see e.g., ref. (4)], which indicates that series resistance only has a minor role in causing the observed frequency dispersion.
- *Recombination-controlled tunneling (9):* in this model, further discussed below, the parallel conductance is large when, at positive gate biases, the

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metal Fermi level lines up with a large density of interface states in the middle of the $In_{0.53}Ga_{0.47}As$ band gap.

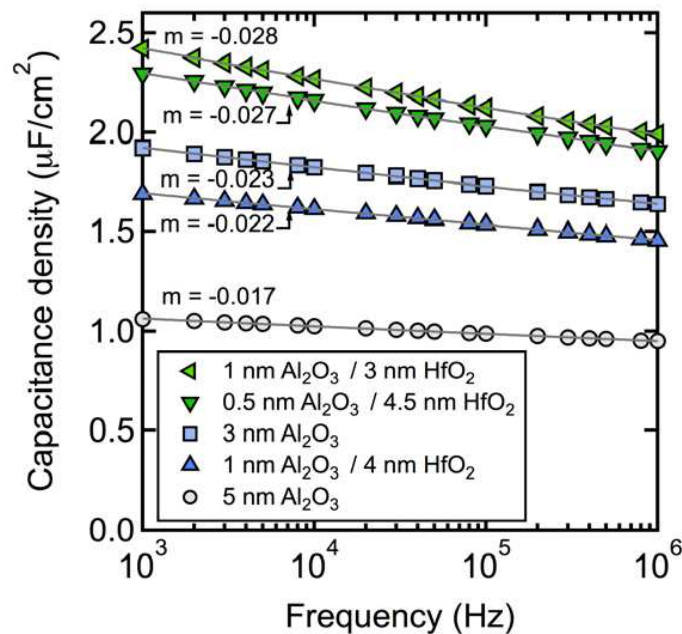

Figure 2: Accumulation capacitance density at V_{FB} + 1 V (V_{FB} is the flatband voltage) as a function of frequency for $Al_2O_3/In_{0.53}Ga_{0.47}As$ and $HfO_2/Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs. The solid lines are a power law fit ($C_{acc} = cf^m$, where C_{acc} is the accumulation capacitance density, c is a constant, f the frequency and m is the power law exponent). The value of m is indicated for each trace.

In the recombination-controlled tunneling model the parallel conductance is large and frequency dependent when interface traps can communicate with the metal via tunneling, which requires that the dielectric is sufficiently thin (10,11). In particular, at positive gate biases, the metal Fermi level lines up with a large density of interface states in the $In_{0.53}Ga_{0.47}As$ band gap. The ac signal causes the metal Fermi level (E_{fm}) to oscillate through E_t (trap level). A conducting channel (ac loss) is provided through recombination of carriers with the interface states, as indicated by the vertical arrow in Fig. 3. In a recent publication (9), we have shown that the model explains in a semi-quantitative manner the experimentally observed capacitor characteristics, including a peak in parallel conductance/frequency versus log frequency curves at positive gate bias, and the dependence of the frequency dispersion on the dielectric thickness. The interface trap states that are responsible for the frequency dispersion in accumulation reside in the *lower half of the* $In_{0.53}Ga_{0.47}As$ *band gap*, as the metal Fermi level lines up with these states at positive gate biases.

Conclusions

In summary, the high, and non-uniform (with respect to their energy distribution in the band gap) interface trap densities at high-*k*/III-V interfaces can give rise to

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pronounced frequency dispersion phenomena in capacitance-voltage and conductance-voltage measurements as a function of frequency. Tunnel currents through these interface states should not be neglected, as the D_{it} of dielectric/III-V interfaces is orders of magnitude higher than for Si MOSCAPs (rising well into 10^{14} $eV^{-1}cm^{-2}$ near the valence band for $In_{0.53}Ga_{0.47}As$) and the conduction band DOS of III-V semiconductors such as $In_{0.53}Ga_{0.47}As$ is several orders of magnitude lower than that of Si.

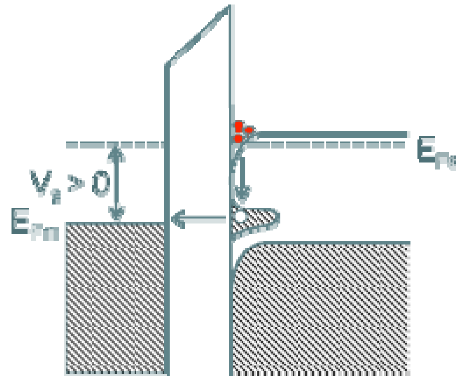

Figure 3: Recombination controlled tunneling process, involving tunneling (horizontal arrow) and electron capture.

Acknowledgments

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