

Modulation of over 10^{14} cm⁻² electrons at the SrTiO₃/GdTiO₃ heterojunction

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The polar discontinuity^[1] and electronic reconstruction at the interface of SrTiO₃ and GdTiO₃ leads to a unique high two dimensional electron gas (2DEG) of 3×10^{14} electron/cm²^[2], that is exactly half of the number of unit cells at the interface. The ability to modulate this high charge density could enable a new class of oxide electronics and plasmonics devices that harness extreme charge density. In this work show how heterostructures field effect transistors can be designed to enable modulation of over 10^{14} cm⁻² electron/cm², where represents the highest charge density modulated in any field effector transistor to date.

Samples were grown on (001)-oriented (LaAlO₃)_{0.3}(Sr₂AlTaO₆)_{0.7} (LSAT) single crystal substrates by molecular beam epitaxy (MBE) using a metal organic precursor (titanium isopropoxide)^[4]. Due to the staggered band line-up between GTO and STO, a 2D electron gas channel is expected to be formed in the wider bandgap STO layer, with an expected sheet charge density of 3×10^{14} cm⁻² (fig. 2). The inverted STO/GTO HFET structure provides the advantage of having STO cap layer with its higher band gap and breakdown strength.

Following optical photolithography technology, metallization for the Ohmic contacts were done using an e-beam evaporated Al/Ni/Au (20/40/200 nm) multilayer stack. Mesa isolation was done using ICP-RIE plasma based on Cl₂/BCl₃ chemistry, followed by e-beam evaporation of Ag/Au (20/200 nm) gate contacts.

To reduce the effect of interfacial layer, we varied the thickness of STO layer (28nm, 40nm and 98nm). Device structure is shown in fig. 1a. As total gate capacitance is the series combination of STO capacitance and interfacial capacitance, effect of interfacial layer could be reduced by lowering the capacitance of STO layer. So HFET with thicker STO layer should have interfacial layer effect minimum and should exhibit higher effective dielectric constant. In fig. 3, capacitance-voltage (C-V) characteristics are shown for different STO thickness. For 98nm STO HFET we found charge modulation of 1.04×10^{14} cm⁻² from CV profile. I_D-V_{DS} profile (fig. 4) also shows around 35% modulation into current that also represents around 1×10^{14} cm⁻² charge modulation under gate.

However, in thick STO HFETs background doping might play some role beside 2DEG. For this reason, we used MBE grown high-k dielectric cap layer of BaSrTiO₃ (BST) ($\epsilon_r \approx 1000$) on top of a thin (20nm) STO layer (fig. 1b). This high-k layer improves gate leakage (fig. 5) as well as effective dielectric constant of cap layer. The C-V profile is shown in fig. 6 and it represents a charge modulation of 9×10^{13} cm⁻². I_D-V_{DS} characteristic (fig. 7) also shows the same magnitude of charge modulation. So BST layer enables the modulation of almost same magnitude of that of thick STO/GTO HFET but with a very thin STO layer. The result is summarized in fig. 8 showing the change of charge modulation with STO thickness.

In conclusion, we developed two different techniques to improve charge modulation in STO/GTO HFET, and we observed record high charge modulation (10^{14} cm⁻²) using this technique. The ability to modulate such high charge density could enable a new class of extreme electron concentration heterostructure devices for electronic, plasmonic, and optoelectronic applications

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References

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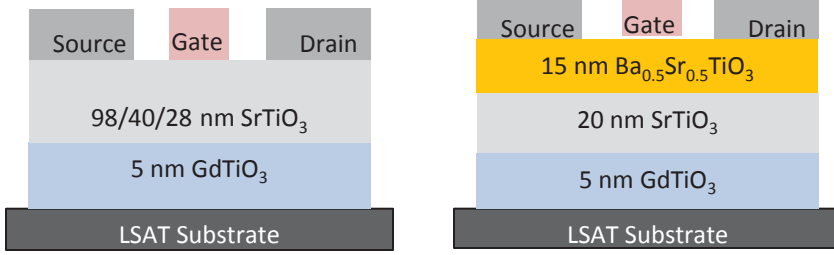


Fig. 1 – Device structure a) STO/GTO HFET b) STO/GTO HFET with high-k BST layer

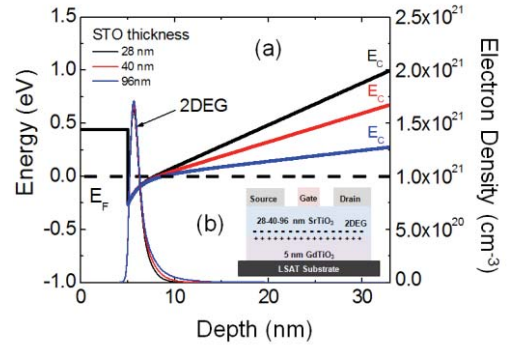


Fig. 2 – Band diagram and charge profile of STO/GTO hetero structure

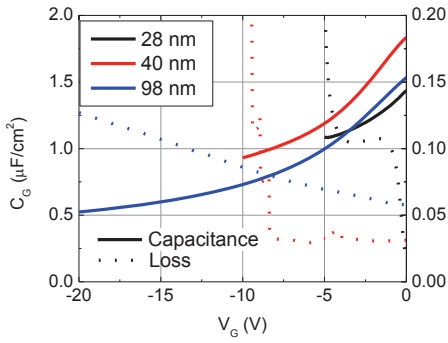


Fig. 3 – Capacitance-Voltage characteristics of STO/GTO HFET for different STO thickness

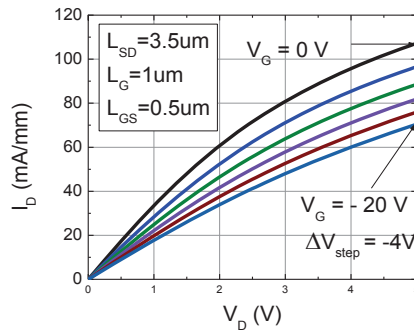


Fig. 4 – I_D - V_{DS} profile for 98nm STO/GTO HFET

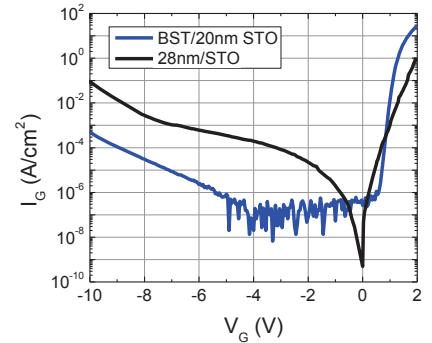


Fig. 5 – Gate leakage comparison for STO/GTO structures with (blue) and without (black) BST layer

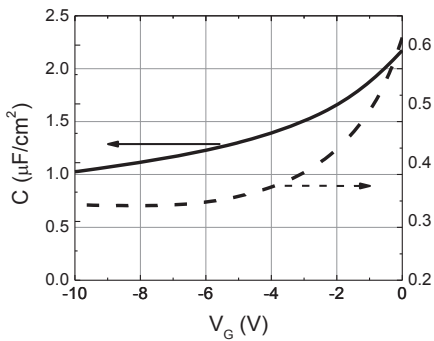


Fig. 6 – Capacitance-voltage characteristic of STO/GTO HFET with BST layer

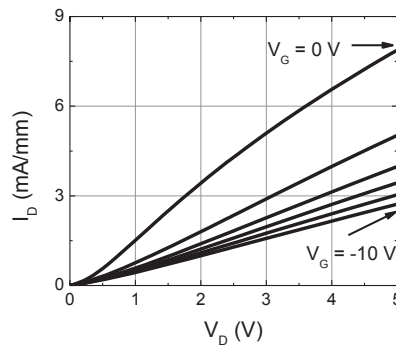


Fig. 7 – I_D - V_{DS} profile for STO/GTO HFET with BST layer

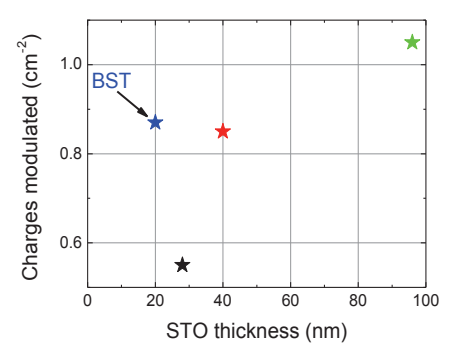


Fig. 8 – Change in charge modulation with STO thickness and effect of BST layer (blue)