Trapping Effects in Si $\delta$-Doped $\beta$-$\text{Ga}_2\text{O}_3$ MESFETs on an Fe-Doped $\beta$-$\text{Ga}_2\text{O}_3$ Substrate

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Abstract—Threshold voltage instability was observed on $\beta$-$\text{Ga}_2\text{O}_3$ transistors using double-pulsed current–voltage and constant drain current deep level transient spectroscopy (DLTS) measurements. A total instability of 0.78 V was attributed to two distinct trap levels, at $E_C$-0.70 and $E_C$-0.77 eV, which need to be mitigated for future applications. The traps are likely located near the gate–drain edge and below the delta-doped layer, which is determined through the DLTS technique and an understanding of the fill and empty biasing conditions. The trap modulation was consistent with a gate leakage-based trap filling mechanism, which was demonstrated. It is likely that Fe is playing a role in the observed dispersion due to the close proximity of the Fe substrate.

Index Terms—Gallium oxide, MESFETs, trapping effects, $V_T$ instability.

I. INTRODUCTION

GALLIUM oxide in its beta phase has received a lot of attention recently for potential applications in high voltage and high frequency devices due to its wide bandgap of $\sim$4.8 eV and theoretical breakdown field of $\sim$8 MV/cm, leading to a $\sim$4× increase in the Baliga figure of merit compared to GaN [1]. $\beta$-$\text{Ga}_2\text{O}_3$ also offers the advantage of growing large area bulk substrates from inexpensive melt methods [2]–[5]. Bulk crystalline substrate availability enables homoepitaxy which supports low concentrations of crystallographic defects, such as threading dislocations, compared to growth on lattice-mismatched substrates. There are limited experimental studies on defects in $\beta$-$\text{Ga}_2\text{O}_3$ [6]–[12], and even fewer discussing the device level impact of traps. $\beta$-$\text{Ga}_2\text{O}_3$ material studies by K. Irmscher et al. and Z. Zhang et al. identified three distinct trap levels in UID (100) and (010) bulk substrates in the upper part of the bandgap at approximately $E_C$-0.6 eV, $E_C$-0.8 eV, and $E_C$-1.0 eV using deep level transient spectroscopy (DLTS) as well as deeper states using deep level optical spectroscopy (DLOS) [6], [7]. In spite of the general lack of comprehensive knowledge on defects thus far, there has been significant progress in $\beta$-$\text{Ga}_2\text{O}_3$ transistor device designs and performance [13]–[19]. However, the effects of specific traps on transistors are still not well understood. Traps in transistors can affect the terminal characteristics such as threshold voltage ($V_T$) and on-resistance ($R_{on}$). It is important to understand trap levels and identify their source to mitigate their effect and improve performance. To shed light on this topic, this study focuses on the impact of deep level traps on the threshold voltage. It is important to note that previous materials defect studies assess traps in films, but it can be difficult to quantify their impact on device characteristics from that information alone.

To assess the effects of traps on the transistor terminal characteristics, double-pulsed current-voltage (I-V) measurements are used to observe the magnitude of the total dispersion given different quiescent conditions. The trap filling is consistent with a gate leakage-based mechanism for this device. Additionally, gate-controlled constant drain current DLTS (GC CID-DLTS) is used to directly identify each trap (trap energy, cross section, and concentration). GC CID-DLTS has the benefit of performing measurements on the transistor allowing the dispersion to be quantitatively associated with specific traps, which then can be correlated with crystalline defects.

II. DEVICE STRUCTURE AND EXPERIMENTAL PROCEDURE

The studied device structure is shown in Fig. 1. This design is promising for laterally scaled devices with high gate-channel capacitance along with higher mobility due to reduced scattering compared to thick channels [20]–[22]. The devices were grown at 700°C in an oxygen plasma-assisted molecular beam epitaxy system in a slightly oxygen-rich condition, resulting in a 3.3 nm/min Ga limited growth rate. Low resistance Ohmic contacts of 1.5 Ω mm were formed by etching past the channel, selectively re-growing a heavily doped $\beta$-$\text{Ga}_2\text{O}_3$, depositing Ti/Au/Ni source and drain contacts, and annealing the contacts for one minute at 470 °C in an N$_2$ atmosphere. After the Ohmic contacts were created, plasma etching was
done for mesa isolation. Ni/Au/Ni Schottky gate contacts with dimensions of 100 μm × 3 μm were deposited through lift-off patterning using optical lithography. Complete growth and processing details can be found in work by Z. Xia et al. [23].

Double pulsed I-V is often used to minimize self-heating through zero bias quiescent conditions ($V_{GS,q} = V_{DS,q} = 0.0$ V). It can also be used to control the trap occupation state given appropriate quiescent conditions. To study the impact of traps on the threshold voltage, two different quiescent conditions, a zero bias and a pinch-off high-$V_{DS}$ bias, were used to acquire the transfer characteristics using a Keithley 4200-SCS with two fast pulse modules. In general, to get an accurate measurement of trap-induced dispersion, the measurement pulse should be at least 10X faster than the fastest trap emission while remaining in the saturation region. In constant drain current DLTS, the majority carrier emission was considered for the process as well, but the trap spectroscopy will reveal that electron traps can fully explain these effects. Hole traps were being trapped thereby reducing the channel charge. Hole emission was considered for the process as well, but the trap spectroscopy will reveal that electron traps can fully explain these effects. Hole traps were being trapped thereby reducing the channel charge.

III. RESULTS AND DISCUSSION

Four devices were tested on this sample and all exhibited similar characteristics, so a representative device is shown in this work. Double-pulsed I-V characteristics in Fig. 2 show the dispersion between the zero bias quiescent ($V_{GS,q} = V_{DS,q} = 0.0$ V) and high-$V_{DS}$ off-state ($V_{GS,q} = -5.0$ V, $V_{DS,q} = 15.0$ V) quiescent biasing conditions. Pulsed I-V revealed that the traps were empty under the zero bias quiescent condition and filled in the high-$V_{DS}$ condition because in the high-$V_{DS}$ condition the $V_T$ shifted +0.78 V which was confirmed through four different methods. The $V_T$ shift was determined by measuring $\Delta V_{GS}$ at $I_D = 1.5$ and 4.0 mA/mm and by linearly fitting the transconductance and transfer curves. All four methods were within ±0.04 V even with high gate leakage current around 100 μA/mm at $V_{DS} = 15$ V in the off-state. This positive $V_T$ shift indicates that electrons were being trapped thereby reducing the channel charge. Hole emission was considered for the process as well, but the trap spectroscopy will reveal that electron traps can fully explain this process. This $V_T$ shift corresponded to a channel electron concentration reduction of $2.2 \times 10^{12}$ cm$^{-2}$ using (1). This large $V_T$ shift is undesirable and identifying the conditions that modulate trap occupancy and the physical location and source of the trap levels is important to understand.

To understand the filling mechanisms for the observed traps, pulsed measurements were performed at different gate bias stresses to determine how $V_T$ depended on previously applied voltages. The stress was applied by grounding the drain and source and applying a gate bias for 100 ms. Then the gate bias was dynamically controlled to maintain $I_D = 1.5$ mA/mm at $V_{DS} = 2.0$ V. This gate bias was compared with the initial threshold voltage to determine $\Delta V_T$, which is shown in Fig. 3a. The $V_T$ instability did not appear until $V_{GS} \geq V_T$ was applied, which indicates that this is unlikely to be a surface state effect. Considering this as a buffer trap, dispersion was not observed when $V_{GS} \geq V_T$ was applied because the channel screened the electric fields below the channel preventing them from reaching the buffer.

To understand the results in Fig. 3a, TCAD modeling using Silvaco Atlas was done. Figure 3b and Fig. 3c show the difference in the field profiles where the fields were shielded.

**Fig. 1.** Cross-sectional diagram of the grown and processed MESFET. The dashed line represents the silicon δ-doping channel. The Ohmic contacts utilize an MBE regrown heavily doped region to reduce contact resistance to the channel and metal.

**Fig. 2.** Transfer characteristics using double pulsed I-V with a zero bias and pinched-off, high-$V_{DS}$ quiescent conditions where a 0.78 V threshold voltage shift between the two conditions is observed. The inset shows the transconductance, $g_m$, curves plotted vs. $V_{GS}$-$V_T$ to show that the shape of the $g_m$ curves is same for both quiescent conditions indicating there is negligible change in the source access resistance.
charge trapped in this layer could contribute to the $V_T$ instability observed in the pulsed I-V. (b) shows the Arrhenius plot used to extract the trap energy and capture cross section, $\sigma_n$, for this sample as well as previous results on bulk Schottky samples from [6] and [7].

Previously published results are also plotted in Fig. 4b to compare the bulk samples and this MESFET grown on an Fe-doped substrate [6], [7]. The transistor showed a similar trap near the previously reported $E_C-0.80$ eV trap level [6], [7], but there was a newly observed trap at $E_C-0.70$ eV that was larger than the $E_C-0.77$ eV peak, indicating that this $E_C-0.70$ eV trap was the dominating level. There are few reports of trapping effects with Fe-doped $\beta$-Ga$_2$O$_3$, and the presence of these observed levels in a MESFET on an Fe-doped substrate suggests the Fe could be playing a role in either the $E_C-0.70$ or the $E_C-0.77$ eV levels. Recent work indicates that Fe may be related to the $E_C-0.77$ eV level [8], and further work is underway to confirm the source of each level as well as the Fe-doped substrate’s effect on the observed $V_T$ dispersion.

The $V_T$ instability observed in this work would potentially be mitigated by reducing the trap concentrations of the $E_C-0.70$ and $E_C-0.77$ eV traps through optimized growth and by keeping Fe impurities far from the channel. Alternatively, the instability may be reduced through minimizing the gate leakage current, which is the proposed trap filling mechanism. However, device degradation may result in increased gate leakage and $V_T$ instabilities might emerge causing parametric device failure. Optimized structure designs and growths would provide a more reliable solution to trap related $V_T$ instabilities. The results presented here provide a guide to improving future buffer designs for minimal dispersion and high-performance devices.

**IV. CONCLUSION**

A transistor level trap study using double-pulsed I-V and GC ClD-DLTS revealed two trap levels in the upper part of the bandgap at $E_C-0.70$ eV and $E_C-0.77$ eV in an MBE grown $\beta$-Ga$_2$O$_3$ MESFET. The pulsed I-V measurements showed a $V_T$ shift only observed after biasing $V_{GS}$ less than $V_T$, where the electric fields extended deep into the buffer and substrate, which was verified through TCAD modeling. The simulated electric field profiles supported the injection of electrons due to gate leakage to enable filling otherwise empty $E_C-0.70$ and $E_C-0.77$ eV electron traps, which is shown to be the source of the $V_T$ shift. Further work is underway to understand the physical sources of the trap levels as well as the cause for the gate leakage in order to mitigate the $V_T$ instability.

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